AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated hereafter.

Claims:

1-18. (Cancelled)

19. (Original) A multi-level, multi-bit stacked gate flash memory cell structure comprising:

floating gate spacers having convex walls facing each other, and vertical outside walls;

a conformal dielectric layer covering said convex walls of said floating gate spacers;

a control gate therebetween said convex walls of said floating gate spacers with intervening said conformal dielectric layer, and

insulative spacers formed on said vertical outside walls of said floating gates.

20. (Original) The stacked gate flash memory cell of claim 19, wherein said floating gate spacers comprise polysilicon having a lateral thickness between about 500 to 2000 Å.

21. (Previously Presented) The stacked gate flash memory cell of claim 19, wherein said conformal dielectric layer comprises oxide-nitride-oxide (ONO) having a thickness between about 150 to 250 Å.

22. (Original) The stacked gate flash memory cell of claim 19, wherein said control gate comprises polysilicon.

23. (Original) The stacked gate flash memory cell of claim 19, wherein said oxide spacers have a lateral thickness between about 1000 to 3000 Å.

24-28. (Cancelled)

29. (Previously Presented) A multi-level, multi-bit stacked gate flash memory cell structure, comprising:

two floating gates on an insulating layer on a substrate, having opposite sidewalls facing each other;

a conformal dielectric layer covering opposite sidewalls of the two floating gates;

a control gate therebetween the opposite sidewalls of the two floating gates with intervening the conformal dielectric layer;

two insulative spacers covering outside walls of the two floating gates; and

further comprising a first, second and third doped regions in the substrate as source/drain regions, wherein the first doped region is disposed between the two opposite sidewalls of the two floating gates, and the second and third doped regions are disposed outside of the outside walls of the two floating gates respectively.

30. (Previously Presented) The flash memory cell structure of claim 29, wherein the substrate is a p-type semiconductor substrate and the first, second and third doped regions are n-doped regions, and the first n-doped region is served as a source region and the second and third n-doped regions are served as a drain regions.

31. (Previously Presented) The flash memory cell structure of claim 29, wherein the floating gates and control gate comprise polysilicon.

32. (Previously Presented) The flash memory cell structure of claim 29, wherein the conformal dielectric layer comprises oxide-nitride-oxide (ONO).